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10/627,468	07/25/2003	Tyler A. Lowrey	MI22-2348	3229

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EXAMINER
KENNEDY, JENNIFER M

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,468	LOWREY ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *78-97* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *78-97* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/04, 7/25/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 80 is objected to because of the following informalities: In line 1 of the claim the examiner believes –the—should be inserted prior to "dielectric barrier". Appropriate correction is required.

Claim 93 is objected to because of the following informalities: In line 7, the examiner believes that "elevational" should be replaced with –elevationally--.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 78, 93, 95, and 97 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In Claim 78, lines 8-9 of the claim recites that the "dielectric layer is exposed relative to said second capacitor electrode". It is unclear by what is meant by the phrase. Is the dielectric exposed to a greater degree relative to the exposure of the second electrode? Is the dielectric layer exposed by removing the portions of second capacitor electrode? The examiner believes that the Applicants intended on reciting that the something to the effect of –removing the second capacitor electrode so as to expose the dielectric--. Examination will be made accordingly.

In Claim 93, lines 3-4 and 6-7 of the claim recites that the " the first and second capacitor electrodes comprising respective uppermost surfaces relative the substrate" and "the dielectric layer comprising an uppermost surface relative the substrate", respectively. It is unclear by what is meant by these phrases. If the first and second capacitor electrodes are the uppermost surface, how then is the dielectric also the uppermost surface? Perhaps Applicants intended on reciting that the first and second capacitors are the uppermost surface at this point during construction and then by forming the dielectric it becomes the uppermost surface. With respect to the dielectric layer recitation, is the claim referring to the uppermost surface of the dielectric that is formed near the substrate? Or is this simply referring to the substrate as the lowermost portion, and thus the uppermost portion of the dielectric would be that furthest from the substrate. Clarification is requested.

In Claim 95 and 97, in lines 1-2 and lines 1-4, respectively of the claim recites that "a first insulative layer elevationally below and contacting the uppermost surface of the dielectric layer". It is unclear how a layer can contact the uppermost surface of a layer it is formed beneath. The examiner requests clarification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

> applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 78-97 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeng et al. (U.S. Patent No. 6,184,081).

In re claim Jeng et al. disclose the method of forming capacitors on a semiconductor device having a substrate, comprising the steps of:

forming a first capacitor electrode (14, 19, 20) supported by said substrate, said first capacitor electrode having a portion which extends generally vertically relative to said substrate;

forming a dielectric layer (22) over said first capacitor electrode;

forming a second capacitor electrode (23a) over a portion of said dielectric layer such that an other portion of said dielectric layer is exposed relative to said second capacitor electrode (see Figure 8); and

forming a dielectric barrier (30) over said exposed portions of said dielectric layer.

In re claim 79, Jeng et al. discloses the method wherein the exposed portion of said dielectric layer comprises an uppermost portion of said dielectric layer (see Figure 8).

The examiner notes that uppermost is read as the topmost or upper or top portion of a layer. Therefore, the dielectric exposed in contact hole 27b can be considered the uppermost portion, or the portion exposed in contact hole 26b can be

considered the uppermost portion since it is the upper portion of the storage electrode (14, 19, 20).

In re claim 80, Jeng et al. discloses the method wherein the dielectric barrier (30) extends at least in part above said first capacitor electrode, said dielectric layer and said second capacitor electrode (see Figure 9).

In re claim 81, Jeng et al. discloses the method further comprising the steps of forming an opening (26b) in said dielectric barrier and forming a conductive element (32) extending into said opening to form an electrically conductive contact to said second capacitor electrode.

In re claim 82, Jeng et al. disclose the method wherein said exposed portion of said dielectric layer comprises an uppermost portion of said capacitors (see Figure 9).

In re claim 83, Jeng et al. disclose the method wherein said exposed portion of said dielectric layer is spaced apart from said first capacitor electrode (see Figure 8, horizontal surface of 22, exposed through 26b).

In re claim 84, Jeng et al. disclose the method wherein the exposed portion of said dielectric layer is spaced apart from and directly over said first capacitor electrode (see Figure 8, horizontal surface of 22, exposed through 26b).

In re claim 85, Jeng et al. disclose the method further comprising insulative material (15) elevationally below and contacting said exposed portion of said dielectric layer.

In re claim 86, Jeng et al. disclose the method wherein the exposed portion of said dielectric layer is spaced apart from the first capacitor electrode, and wherein said dielectric layer comprises other portions contacting said first capacitor electrode (see Figure 8, horizontal surface of 22, exposed through 26b).

In re claim 87, Jeng et al. disclose the method wherein at least one of said first and second capacitor electrodes extends substantially vertically relative said substrate (23b, see Figure 8).

In re claim 88, Jeng et al. disclose the method of manufacturing a semiconductor device having capacitors thereon, comprising the steps of:

forming first and second capacitor (14, 19, 20) electrodes supported by a semiconductor substrate, each said capacitor electrode having a portion extending vertically relative to said substrate, said first and second electrodes electrically isolated from each other (see Figure 5);

forming a first dielectric layer (22) extending over at least a portion of both of said first and second electrodes, said first dielectric layer extending over at least an uppermost portion of each of said first and second electrodes (see Figure 6);

forming a conductive layer (23a) extending over said first dielectric layer and above said first and second electrodes;

selectively removing selected portions of said conductive layer to expose a first portion of said first dielectric layer relatively proximate said substrate (bottom/side portion of horizontal portion of 22, see Figure 8), and to expose second and third

portions of said first dielectric layer relatively remote from said substrate (top portion of horizontal portion of 22 exposed, see Figure 8), and to electrically isolate sections of said conductive layer to form a third capacitor electrode (23b) in contact with a portion of said first dielectric layer proximate said first electrode, and a fourth capacitor electrode (23b) in contact with a portion of said first dielectric layer proximate said second electrode, said third and fourth capacitor electrodes electrically isolated from one another; and

forming a second dielectric layer (30) over said exposed portions of said first dielectric layer and over said third and fourth electrodes.

The examiner notes that uppermost is read as the topmost or upper or top portion of a layer. Therefore, the dielectric exposed in contact hole 27b can be considered the uppermost portion, or the portion exposed in contact hole 26b can be considered the uppermost portion since it is the upper portion of the storage electrode (14, 19, 20). For instance, in one interpretation, knowing that more than one device would be formed on the substrate, Jeng et al. disclose selectively removing selected portions of said conductive layer to expose a first portion of said first dielectric layer relatively proximate said substrate (horizontal portion of 22 exposed by contact hole 26b, see Figure 8), and to expose second and third portions of said first dielectric layer relatively remote from said substrate (top portion of vertical portion of 22 exposed in contact hole 27b, see Figure 8).

Alternatively, in another interpretation, Jeng et al. disclose selectively removing selected portions of said conductive layer to expose a first portion of said first dielectric layer relatively proximate said substrate (bottom/side portion of vertical portion of 22 exposed in contact hole 27b, see Figure 8), and to expose second and third portions of said first dielectric layer relatively remote from said substrate (top portion of vertical portion of 22 exposed in contact hole 27b, see Figure 8). Furthermore, the examiner notes that the terms relatively remote and relatively proximate are broad. The examiner reads these terms to require one portion to be closer to the substrate and one portion to be further from the substrate.

In yet another interpretation, Jeng et al. disclose selectively removing selected portions of said conductive layer to expose a first portion of said first dielectric layer relatively proximate said substrate (bottom/side portion of horizontal portion of 22, see Figure 8), and to expose second and third portions of said first dielectric layer relatively remote from said substrate (top portion of horizontal portion of 22 exposed, see Figure 8). Furthermore, the examiner notes that the terms relatively remote and relatively proximate are broad. The examiner reads these terms to require one portion to be closer to the substrate and one portion to be further from the substrate.

In re claim 89, Jeng et al. disclose the method further comprising the step of forming a conductive line (32) extending through said second dielectric layer (30) and contacting said third and fourth capacitor electrodes to establish electrical communication between said capacitor electrodes.

In re claim 90, Jeng et al. disclose the method wherein said second dielectric layer (see Figure 9) is in contact with said first dielectric layer and with said third and fourth capacitor electrodes.

In re claim 91, Jeng et al. disclose the method wherein said second and third portions of said first dielectric layer comprise and uppermost portion of said capacitors. The examiner notes that uppermost is read as the topmost or upper or top portion of a layer. Therefore, the dielectric exposed in contact hole 27b can be considered the uppermost portion, or the portion exposed in contact hole 26b can be considered the uppermost portion since it is the upper portion of the storage electrode (14, 19, 20).

In re claim 92, Jeng et al. disclose the method wherein said second and third portions of said first dielectric layer are spaced apart from respective said first and second capacitor electrodes (horizontal portions of dielectric 22).

In re claim 93, Jeng et al. disclose the method of forming capacitors, comprising:

forming first and second capacitor electrodes supported by a substrate, the first and second capacitors electrode comprising respective uppermost surfaces relative the substrate (14, 19, 20); and

forming a dielectric layer (22) disposed between the first and second capacitor electrode, the dielectric layer comprising an uppermost surface relative the substrate, the uppermost surface of the dielectric layer being elevationally above one of the

uppermost surface of the first and second capacitor electrodes and being coextensive with the other of the uppermost surfaces of the first and second capacitor electrodes.

In re claim 94, Jeng et al. disclose the method wherein at least one of the first and second capacitor electrodes is oriented substantially vertically relative the substrate (see Figure 8).

In re claim 95, Jeng et al. disclose the method further comprising insulative material (15) elevationally directly below and contacting the uppermost surface of the dielectric layer.

In re claim 96, Jeng et al. disclose the method further comprising insulative material (30) elevationally directly above and contacting the uppermost surface of the dielectric layer.

In re claim 97, Jeng et al. disclose the method further comprising a first insulative (15) layer elevationally below and contacting the uppermost surface of the dielectric layer, and further comprising a second insulative layer (30) elevationally above and contacting the uppermost surface of the dielectric layer.

Claims 78-97 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura (U.S. Patent Appl. 2001/0044181).

I In re claim disclose the method of forming capacitors on a semiconductor device having a substrate, comprising the steps of:

forming a first capacitor electrode (46) supported by said substrate, said first capacitor electrode having a portion which extends generally vertically relative to said substrate (see Figure 3C);

forming a dielectric layer (52) over said first capacitor electrode;

forming a second capacitor electrode (56) over a portion of said dielectric layer such that an other portion of said dielectric layer is exposed relative to said second capacitor electrode (see Figure 4A); and

forming a dielectric barrier (64, see Figure 5A) over said exposed portions of said dielectric layer.

In re claim 79, discloses the method wherein the exposed portion of said dielectric layer comprises an uppermost portion of said dielectric layer (see Figure 4A).

In re claim 80, discloses the method wherein the dielectric barrier extends at least in part above said first capacitor electrode, said dielectric layer and said second capacitor electrode (see Figure 5A).

In re claim 81, discloses the method further comprising the steps of forming an opening in said dielectric barrier and forming a conductive element (60) extending into said opening to form an electrically conductive contact to said second capacitor electrode (see Figure 5B).

In re claim 82, disclose the method wherein said exposed portion of said dielectric layer comprises an uppermost portion of said capacitors (see Figure 4A).

In re claim 83, disclose the method wherein said exposed portion of said dielectric layer is spaced apart from said first capacitor electrode (see Figure 4A, extends vertically away and apart from first capacitor electrode).

In re claim 84, disclose the method wherein the exposed portion of said dielectric layer is spaced apart from and directly over said first capacitor electrode (see Figure 4A, 52 extends vertically away and apart from first capacitor electrode).

In re claim 85, disclose the method further comprising insulative material (58) elevationally below and contacting said exposed portion of said dielectric layer.

In re claim 86, disclose the method wherein the exposed portion of said dielectric layer is spaced apart from the first capacitor electrode, and wherein said dielectric layer comprises other portions contacting said first capacitor electrode (see Figure 4A, 52 extends vertically away and apart from first capacitor electrode).

In re claim 87, disclose the method wherein at least one of said first and second capacitor electrodes extends substantially vertically relative said substrate (see Figure 4A).

In re claim 88, disclose the method of manufacturing a semiconductor device having capacitors thereon, comprising the steps of:

forming first and second capacitor electrodes (46, see Figure 3C) supported by a semiconductor substrate, each said capacitor electrode having a portion extending vertically relative to said substrate, said first and second electrodes electrically isolated from each other;

forming a first dielectric layer (52) extending over at least a portion of both of said first and second electrodes, said first dielectric layer extending over at least an uppermost portion of each of said first and second electrodes (see Figure 3C);

forming a conductive layer (56) extending over said first dielectric layer and above said first and second electrodes;

selectively removing selected portions of said conductive layer to expose a first portion of said first dielectric layer relatively proximate said substrate (see Figure 4A, right hand side, 52, exposed, then later covered with 58, and Figure 6B), and to expose second and third portions (see Figure 4A, left hand side, topmost portions of 52 exposed, and Figure 6B) of said first dielectric layer relatively remote from said substrate, and to electrically isolate sections of said conductive layer to form a third capacitor electrode in contact with a portion of said first dielectric layer proximate said first electrode, and a fourth capacitor electrode in contact with a portion of said first dielectric layer proximate said second electrode, said third and fourth capacitor electrodes electrically isolated from one another (see Figure 4A, and [0131], [0151]); and

forming a second dielectric layer (64) over said exposed portions of said first dielectric layer and over said third and fourth electrodes.

In re claim 89, disclose the method further comprising the step of forming a conductive line extending (60) through said second dielectric layer and contacting said third and fourth capacitor electrodes to establish electrical communication between said capacitor electrodes.

In re claim 90, disclose the method wherein said second dielectric layer(64) is in contact with said first dielectric layer and with said third and fourth capacitor electrodes (see Figure 5A).

In re claim 91, disclose the method wherein said second and third portions of said first dielectric layer comprise and uppermost portion of said capacitors (see Figure 4A and Figure 6B).

In re claim 92, disclose the method wherein said second and third portions of said first dielectric layer are spaced apart from respective said first and second capacitor electrodes (see Figure 4A, Figure 6B, 52 extends vertically away and apart form first and second capacitor electrodes).

In re claim 93, disclose the method of forming capacitors, comprising:

forming first and second capacitor electrodes (46) supported by a substrate, the first and second capacitors electrode comprising respective uppermost surfaces relative the substrate; and

forming a dielectric layer (52) disposed between the first and second capacitor electrode, the dielectric layer comprising an uppermost surface relative the substrate, the uppermost surface of the dielectric layer being elevationally above one of the uppermost surface of the first and second capacitor electrodes and being coextensive with the other of the uppermost surfaces of the first and second capacitor electrodes.

In re claim 94, disclose the method wherein at least one of the first and second capacitor electrodes is oriented substantially vertically relative the substrate (see Figure 4A).

In re claim 95, disclose the method further comprising insulative material (24) elevationally directly below and contacting the uppermost surface of the dielectric layer.

In re claim 96, disclose the method further comprising insulative material elevationally directly above (64) and contacting the uppermost surface of the dielectric layer.

In re claim 97, disclose the method further comprising a first insulative layer elevationally below (24) and contacting the uppermost surface of the dielectric layer, and further comprising a second insulative layer elevationally above (64) and contacting the uppermost surface of the dielectric layer.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Prall et al. (U.S. Patent No. 6,274,423) discloses the claimed method of forming capacitors when broadly interpreted in a similar manner to that of Jeng et al. (U.S. Patent No. 6,184,081).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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jmk